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PATENT  
Docket No. INTEL/17225

**IN THE UNITED STATES PATENT  
AND TRADEMARK OFFICE**

Applicants:	)	I hereby certify that this paper and the
	)	documents referred to as enclosed
<b>TIAN et al.</b>	)	therewith are being deposited with the
	)	United States Postal Service as first
U.S. Serial No.: 10/677,414	)	class mail, postage prepaid, in an
	)	envelope addressed to Commissioner
For: "Methods and Apparatus for	)	for Patents, P.O. Box 1450,
Reducing Memory Latency	)	Alexandria, Virginia 22313-1450 on
in a Software Application"	)	this date:
	)	
Filed: October 2, 2003	)	<b>October 14, 2004</b>
	)	
Assignee: Intel Corporation	)	
	)	Mark C. Zimmerman
Group Art Unit: 2121	)	Attorney for Applicant(s)
	)	Registration No. 44,006
Examiner: Not Yet Assigned	)	

**STATUS LETTER**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

Sir:

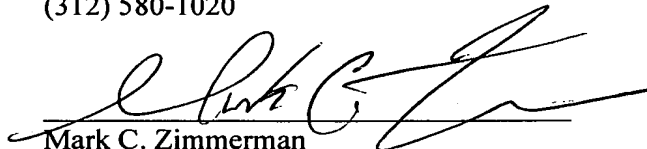
Kindly advise when an Office action can be expected in the above-referenced matter.

Respectfully submitted,

GROSSMAN & FLIGHT, LLC  
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**October 14, 2004**

By:

  
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Attorneys for Intel Corporation